

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	((("6272151") or ("4963768")).PN.	USPAT	OR	OFF	2005/08/18 18:17
L2	742	(703/13,28).CCLS.	USPAT	OR	OFF	2005/08/18 18:19
L3	674	i960	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 18:19
L4	14	3 and prototype	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 18:31
L5	95	cyclone.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 18:31
L6	0	5 and fpga	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 18:31
L7	2	5 and (circuit adj board)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 18:37
L8	1	thomson.xa. and "8051" and emulation and dsp	USPAT	OR	OFF	2005/08/18 18:41
L9	30	("4992934"   "5283900"   "5291614"   "5313618"   "5329471"   "5438672"   "5442789"   "5450607"   "5481684"   "5481693"   "5574927"   "5630153"   "5748468"   "5761516"   "5781792"   "5790824"   "5799169"   "5819067"   "5872993"   "6032247"   "6052773"   "6163764"   "6185522"   "6185628"   "6223274"   "6256725"   "6272452"   "6308255"   "6374312").PN. OR ("6564179"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/18 18:42

L10	1	9 and fpga	USPAT	OR	OFF	2005/08/18 18:42
L11	54	( "4336601"   "4354228"   "4493029"   "4594661"   "4700187"   "4748585"   "4771285"   "4791602"   "4870302"   "4879688"   "4918440"   "4969121"   "4992933"   "5019736"   "5027315"   "5038386"   "5081375"   "5301344"   "5315178"   "5336950"   "5352940"   "5361373"   "5379382"   "5426378"   "5737631"   "5742180"   "5748979"   "5752035").PN. OR ("6052773").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/18 18:50
L12	24	11 and fpga	USPAT	OR	OFF	2005/08/18 18:50

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L1	2	((("6272151") or ("4963768"))).PN.	USPAT	OR	OFF	2005/08/18 18:17
L2	742	(703/13,28).CCLS.	USPAT	OR	OFF	2005/08/18 18:18

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L1	1	("5329470").PN.	USPAT	OR	OFF	2005/08/18 16:36
L2	92	acres.in.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/18 16:37
L3	32	2 and video	US-PGPUB; USPAT; USOCR	OR	OFF	2005/08/18 16:41
L4	183	quickturn.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 16:41
L5	143	4 and emulat\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 16:43
L6	55	5 and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 16:43
L7	27	6 and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/18 16:43

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L1	32	quickturn.as. and emulat\$4 and FPGA and processor	USPAT	OR	ON	2005/08/18 17:52
L2	358	FPGA and emulat\$4 and ASIC and (circuit adj board)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:53
L3	344	2 and interface	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:54
L4	289	3 and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:54
L5	169	4 and master	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:54
L6	169	5 and system	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:55
L7	156	6 and (place or route)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/18 17:55

**Inventor Name Search Result**

Your Search was:

Last Name = ABRAHAMSON

First Name = CARL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09820049</a>	Not Issued	071	03/28/2001	DYNAMICALLY ADAPTABLE DIGITAL ARCHITECTURE SYSTEM	ABRAHAMSON, CARL K.
<a href="#">06518645</a>	<a href="#">4523836</a>	250	07/29/1983	CONTINUOUS COPIER	ABRAHAMSON, CARL W.
<a href="#">06279815</a>	<a href="#">4431350</a>	250	07/02/1981	DISARMING APPARATUS	ABRAHAMSON, CARL-HUGO
<a href="#">06118911</a>	<a href="#">4283250</a>	150	02/06/1980	SOLUTION-CONCENTRATING APPARATUS	ABRAHAMSON, CARL-HUGO

**Inventor Search Completed: No Records to Display.**

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R Tessier, J Babb, M Dahl, S Hanono, A Agarwal - 1994 ACM International Workshop on Field-Programmable Gate ... - [ecs.umass.edu](#)

... Wires Emulation System exhibits high **FPGA** gate utilization ... to eliminate the cost of **signal** switching elements ... A system capable of **emulating** 20,000 gates has ...

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R Tessier, J Babb, M Dahl, S Hanono, D Hoki - [cag.lcs.mit.edu](#)

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P Alternatives - [ieeexplore.ieee.org](#)

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J Kampe, G Scarbata, S Arit, U Heiber, M Ponca, A ... - [inf-technik.tu-ilmenau.de](#)

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### An FPGA-based approach for speeding-up Fault Injection campaigns on safety-critical circuits

P Civera, L Macchiarulo, M Rebaudengo, MS Reorda, ... - Journal of Electronic Testing: Theory and Applications, 2002 - [springerlink.com](#)

... Suitable techniques are proposed, allowing **emulating** the effects ... in charge of initializing the **FPGA**, feeding the ... cycle by triggering the inject **signal** at that ...

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### Verification of a Microcontroller IP Core for System-on-a-Chip Designs Using Low-Cost Prototyping ...

S Schmitt, W Rosenstiel - Proceedings of the Design, Automation and Test in Europe ..., 2004 - [ieeexplore.ieee.org](#)

... The task of **emulating** a complex **ASIC** IP core ... hundreds of sig- nals a complex **signal** multiplexing infrastructure ... million system-gates of a XCV2000E **FPGA** can be ...

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H Hakkarainen, J Isoaho - Proc. 8 thAnn. IEEE Int'l **ASIC** Conference and Exhibit - [ieeexplore.ieee.org](#)

... to any synthesis procedure targeted to **FPGA** technology and ... the program memories of the **signal** processors ... Figure 4. The configuration for **emulating** target system ...

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M Courtoy - The 1996 Southcon Conference, 1996 - [ieeexplore.ieee.org](#)

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## Rapid prototyping of a co-processor based engine knock detection system

A Kirschbaum, S Ortmann, M Glesner - PROC INT WORKSHOP RAPID SYST PROTOTYPING. pp. 124-129. 1998, 1998 - doi.ieeecs.org

...the Digital **Signal** Processor, and REPLICA for **emulating** the communication ... synthesize the necessary glue- logic to the **FPGA** on the ... Digital **Signal** Processor (C40 ...

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